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TACTICAL ELECTRONIC RECONNAISSANCE PROCESSING AND EVALUATION SEGMENT A NEW LOOK

Daniel Patrick Kollay

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THESIS

TACTICAL ELECTRONIC RECONNAISSANCE
PROCESSING AND EVALUATION SEGMENT
A NEW LOOK

by

Daniel Patrick Kollay
and
Kenneth Lee Kreutzer

June 1976

Thesis Advisor: N. F. Schneidewind

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With the proposed procurement of EA-6B aircraft, the U. S. Marine Corps planned the development of TERPES (Tactical Electronic Reconnaissance Processing and Evaluation Segment) to perform post-mission tape analysis. The development phase was initiated on a first generation tactical computer, CP-642B. The thrust of this paper was to identify state-of-the-art replacements for the CP-642B, while identifying areas of concern

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20. Abstract (cont.)

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TACTICAL ELECTRONIC RECONNAISSANCE PROCESSING AND EVALUATION SEGMENT A NEW LOOK

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ABSTRACT

With the proposed procurement of EA-6B aircraft, the U.S. Marine Corps planned the development of TERPES (Tactical Electronic Reconnaissance Processing and Evaluation Segment) to perform post-mission tape analysis. The development phase was initiated on a first generation tactical computer, CP-642B. The thrust of this paper was to identify state-of-the-art replacements for the CP-642B, while identifying areas of concern within the development cycle. Alternative systems were discussed with the emphasis on system flexibility and expandability.

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I. INTRODUCTION

Within the electronic warfare community the EA-6A has been commonly referred to as an active jamming platform. It was employed as a stand-off jamming platform, whereby it provided ECM protection for a strike force from a position out of defensive weapons range, or as an integral part of the strike force. Along with this main mission, it was designed to record emmitter characteristics and location plotting information. In the formulative stages of this passive role, the AN/TSQ-90 Ground Data Readout System was tasked with providing digital and analog data analysis of inflight recordings. Operational evaluation of the recorded data provided by the EA-6A recording system has shown that the data is of poor quality and limited quantity. In its present configuration, the AN/TSQ-90 has been unable to effectively produce meaningful and timely analysis of the data as provided to it. Other limitations of the AN/TSQ-90 were the lack of an interactive graphic capability which was required for analyst interface and for mission planning , and the use of a limited local database of electronic emitters.

With the planned acquisition of the EA-6B it was deemed necessary to expand the capabilities of the AN/TSQ-90. The capabilities expansion program will be referred to as TERPES (Tactical Electronic Reconnaissance Processing and Evaluation Segment). TERPES will be a system that encompasses all facets of analysis of intercepted electronic emissions including required personnel, hardware, software, and analysis techniques. The operational goals of TERPES are: (1) pre/post-mission briefing and analysis; (2) flight

crew/analyst training; and (3) the forwarding of data as prescribed by the MAGIS (Marine Air Ground Intelligence System) concept. To operate effectively TERPES must have inputs from airborne collectors in the form of analog and digital tapes. The digital tape will be returned to the TERPES analysis site, for further analysis of: (1) the aircraft flight path; (2) electronic parameter data; and (3) the direction of arrival of radiating emitters. The analog tapes will augment the digital tapes by supplying additional parameter data and the conversations of crewmen during the various phases of electronic countermeasures and electronic support missions.

As a stand-alone system TERPES must have the capability to maintain, update and query the Electronic Order of Battle and the Electronic Parameter List as provided in database form by the Naval Intelligence Processing System. It must also have the ability to enable the construction of data files of past missions and jammer characteristics. Incorporated into TERPES must be the ability to have a man-machine interactive dialogue that will assist in the preparation of intelligence reports and mission planning. This interactive phase will allow for timely and efficient data analysis and reporting which does not currently exist in the AN/TSQ-90 system.

With the establishment of a development task force, it was ascertained that the present system hardware configuration should be preserved as much as possible. The overriding factor to limit system modernization was development deadline dates. By not attempting to update the AN/TSQ-90 hardware the developers were able to limit their technical problems, both in the area of hardware interfacing and software structuring. Another advantage of this approach was to reduce the need for additional personnel training, as the operational user community was capable of handling the

operational and maintenance aspects of TERPES. These arguments were economically sound but the underlying fact of system flexibility will suffer because of them. By choosing not to modernize, the developers have accepted a heavier slower machine that is not flexible enough to handle the software modifications required to fully implement the operational goals of TERPES. The development team's goal was to develop a baseline TERPES on the present hardware with the expressed idea of upgrading the processor and certain associated hardware as the required units became available [1]. The main thrust of this thesis was to examine the alternatives to system expansion which are:

1) Maintain the present system with a planned expansion of core memory to permit a higher degree of multiprogramming.

2) Replace the CP-808 with the AN/UYK-20 when it is available for installation and application software development.

3) Replace the CP-808 with a militarized processor comparable to the AN/UYK-20.

4) Replace the CP-808 with a commercially available state-of-the-art machine.

II. SYSTEM CONFIGURATION

A. HARDWARE

As a functional entity TERPES has two aspects of processing, analog and digital. For this study the aspects of the digital processing hardware have been addressed. The total TERPES hardware configuration is housed in three Navy Standard 20ft by 8ft by 8ft avionics vans enabling the system to be transported by land or by air. The digital shelter is air-conditioned by two units capable of 72,000 BTU's. Power requirements are supplied through a 400 HZ converter which has a 60 HZ source of power.

1. Processor

The central processor, the CP-808, was a lightweight version of the CP-642B digital computer which has been employed in NTDS. The CP-808 consisted of two units, the power supply cabinet and the logic unit. The logic cabinet contained four I/O chassis, five memory chassis, a chassis for control and bootstrap memory and three chassis for control and arithmetic logic. The power supply provided the dc voltages required by the computer through a single power cable.

The CP-808 was classified as a large-scale, general-purpose computer that utilized a stored program architecture. The CP-808 had the capability of communicating

with its peripheral equipment via twelve I/O channels. Channel transfer speeds were either 166,667 30-bit words/sec/channel or 41,667 30-bit words/sec/channel.

The repertoire of computer instructions permitted mathematical operations, peripheral device control, and other data processing functions. Control routines and programs were entered via a punched tape reader or magnetic tape unit. Communication was performed in a parallel mode 30-bits in length.

The CP-808 performed its internal operations using one's complement binary notation in a parallel mode. The word length was 30 bits with addressable half-words being 15 bits in length. [2]

a. Functional Characteristics

(1) Control Section

This section was designed to direct the operations of the other sections of the computer after receiving the pertinent instruction from memory. The control section was further responsible for decoding the instruction in order to specify where the operand was coming from and the operations that must be performed on it. In conjunction with this last point the control section established the timing sequences required to perform the correct operations.

(2) Arithmetic Section

The arithmetic section incorporates the timing circuits, registers, and modifiers required to perform logical or arithmetic functions as they were specified by the instruction word. The registers in this

section contain the data that was to be manipulated and they were further used as a temporary storage location for the result. The registers were 30 bits in length and the capability to form a 60 bit double length word existed between two of the registers.

(3) Input/Output Section

Initiation of I/O commands was performed by either the computer or an associated I/O device. I/O transmission was done via four registers that act as temporary storage locations for all data passed between the computer and the peripheral device with each register handling four channels. All communication between the processor and the devices was asynchronous and any specific data transmission was done in 30-bit parallel mode. As configured, concurrent bi-directional data transmission between the CP-808 and its peripherals via twelve output and twelve input channels was possible. With a buffer of data prepared for transmission a set of control circuits governed the transfer of data, freeing other sections of the computer for further processing.

(4) Memory Section

MAIN MEMORY -- Core memory consisted of 32,608 addressable locations that had a memory cycle time of 4 microseconds. Core memory was primarily used for program and data storage, I/O interrupt registers, and interrupt storage registers.

CONTROL MEMORY -- This segment contained 128 addressable locations that had a cycle time of 400 nanoseconds. This section contained the index registers and I/O buffer control registers.

BOOTSTRAP MEMORY -- The final memory section dealt with 64 words of read only memory with a cycle time of 667 nanoseconds. This section was programmed during the manufacturing cycle and cannot be changed. These programs were initiated from any point in a program and upon execution termination, control was returned to the pre-selected bootstrap program.

b. Major Operational Characteristics

WORD LENGTH	30 BITS
ARITHMETIC	Parallel, One's Complement
MEMORY AVAILABLE	
Core	32,768 Words at 4 Microsecs
Control	128 Words at 400 Nanosecs.
Bootstrap	64 ROM Words at 667 Nanosecs.
COMPUTER WEIGHT	2165.5 Pounds
POWER SUPPLY	150 Pounds
COMPUTER DIMENSIONS	
Height	72 Inches
Width	38 Inches
Depth	37 Inches
CLEARANCE REQUIREMENTS	
Top	7 Inches
Front	22 Inches
Rear	4 Inches
Sides	18 Inches
INSTRUCTION REPERTOIRE	64 Single address, Flexible Instructions with Provisions for Address or Operand Mod by 8 Index Registers.
INPUT/OUTPUT	12 High Speed Parallel Channels
Operating Temperature	0^{o} to 50^{o} C

Overtemperature Warning ...	Alarm/Light at 46° C
Overtemperature Shutdown ..	Power Off at 60° C
Maximum Relative Humidity .	95 Percent
Storage Temperature	-62° to 75° C
POWER REQUIREMENTS	
Logic Circuits	2500 Watts of 3-phase at 115 Volts and 400 cps.
Cooling Fan	2000 Watts of 3-phase at 115 Volts and 400 cps. [2]

2. Direct Access Storage Device

In order to increase the capability of the AN/TSQ-90, it was deemed necessary to increase the availability of high speed memory. At this point it was ascertained that the Control Data Disk Storage Unit would solve the problem as a high speed, random access, data storage device that could be interfaced to the present system. This particular disk was the commercial equivalent of the CDC 9740 with a microprogrammable controller. The Storage Unit was best described by the functions that it performed: (1) getting the disk up to operating speed; (2) positioning the heads at the required cylinder location; and (3) extracting the required data as designated by the controller.

a. Disk Characteristics

RECORDING SURFACES	19
TRACKS/CYLINDER	19
READ/WRITE HEADS	19
AVERAGE ACCESS TIME	35 MS (seek + rotational delay)
MAXIMUM ACCESS TIME	70 MS (seek + rotational delay)
RECORDING DENSITY	1530 BPI (outer track) 2220 BPI (inner track)
DATA TRANSFER RATE	312,500 characters/sec
BITS/CHARACTER	8
BITS/STORAGE UNIT	475,000,000
PHYSICAL SIZE/CABINET	
Height	38 Inches
Width	27 Inches
Depth	37 Inches
Weight	660 Pounds
Disk Surface Coating	Magnetic Oxide [3]

3. Graphical Display

With the thought of analyzing incoming data in an efficient and timely manner the AN/TSQ-90 was expanded to include an interactive graphics display. The graphics terminal that was decided upon was the Motorola Totalscope III. This particular model was a programmable stand-alone version that has a self-contained 8K of 16-bit words of memory. The Totalscope utilized a bus-organized system to link the various assemblies within the display. One assembly was designed to receive data codes, interpret them and provide the control functions that routed the commands to the proper display assembly. The stand-alone capability was

controlled by an internal arithmetic register controller which contained operator interactive functions, test routines, and I/O controller functions. When coupled with a peripheral keyboard, symbol generator, vector generator, lightpen and joystick, the graphical capability needed to update the system to the requirements of TERPES were present.

a. Performance Characteristics

Using reliability prediction measures performed in accordance with MIL-HDBK-217A the graphical display will have a mean-time-between-failure of 2500 hours. The Totalscope was a fully militarized piece of electronic equipment.

RESOLUTION	1024 Elements in both X and Y
LOCATION ACCURACY	±2 Resolution Elements within the 12- by 10- inch viewing area.
VECTOR GENERATION	Fixed rate of .2 in/usec.
CHARACTER REPERTOIRE	128 ASCII Characters
WEIGHT	130 Pounds
DIMENSIONS	
Length	19 Inches
Height	20 Inches
Width	17 Inches [4]

4. Printers

The line printer utilized by TERPES operates with single or multi-copy continuous fanfolded paper at a maximum line rate of 600/minute. It had the capability of

outputting any of 64 characters within the field width of 120 character positions. [1]

In conjunction with the aforementioned line printer, TEEPES utilized an I/O Keyboard Printer Model 1533. This particular device enabled the operator to communicate with the CP-808. As an input device, the operator was capable of entering new programs, altering existing programs, changing input parameters and initiating program execution and termination. As an output device it was used to display error conditions, program listings and requesting required data from the operator. An operator was able to transmit to the computer any of 64 different characters at a rate up to about 100 words per minute. As an output medium, the printer was capable of outputting the same 64 characters as available for input and operate at about the same 100 words per minute rate.

This device was a commercial unit that had been enclosed in a specially designed protective cabinet and mounted on cup-style resilient mounts. [5]

5. Tape Units

The system contained a set of four tape units that were fully militarized and carry the Univac number 1240A. The tape drives were capable of reducing tapes that had a density of 556 BPI. This rate was adequate for use with the EA-6A but it is not totally compatible with the EA-6B. The onboard recorder on the EA-6B had the capability of recording at 200, 556, or 800 BPI. [1] It was determined that a tape unit be procured to handle the three BPI rates available on the EA-6B, in order to provide maximum taping flexibility.

6. Digital Plotter

Intercept plotting within TERPES was performed by a Calcomp Model 563 Digital Incremental Plotter. The Plotter Adapter provided the interface between the CP-808 and the plotter. The adapter was responsible for generating time signals and control commands to insure asynchronous communication with the plotter. The adapter provided this asynchroncus operation by decoding data words from the CP-808 and producing control signals required to properly perform the applicable plotting function.

The Model 563 was a commercial drum-type plotter that was capable of plotting one variable against another. Plot production occurred with the movement of a pen over the chart paper. The X, Y and Z axis of the plotter were implemented through a series of digital signals that directed drum, carriage and pen movements. The bi-directional rotary step motors on the X and Y axis caused the drum or pen carriage to move in increments of .01 inch, .005 inch or .1 mm per step depending on hardware configuration. The rotary step motors operated at a maximum rate of 300 steps/sec.

a. Operating Characteristics

SPEED	Drum Axis: maximum 300 steps/sec for .005-in and .1-mm steps. maximum 200 steps/sec for .01-in steps. Carriage Axis: same as above. Pen: maximum 5 up and 5 down per second.
RESOLUTION	± 1 step on either axis over the entire roll length.
WEIGHT	53 pounds
DIMENSION	
Width	39 inches
Depth	14 inches
Height	9 inches
PAPER SIZE	Roll Chart paper-120 feet long and 39 inches wide. [6]

B. SOFTWARE

The software to support TERPES was in the final stages of development at the Naval Missile Center, Pt. Mugu. The first phase of software design was to interface two new pieces of equipment into the AN/TSQ-90, a disk drive unit and a graphics terminal. These two devices were meant to expand the processing power of the AN/TSQ-90 to meet TERPES specifications while establishing a new dimension, an intervening analyst, in the data reduction cycle.

With the interface complete, it was necessary to establish the software structure required to fully utilize the resources of the expanded hardware suit. Modularity within the software structure was necessary to provide an analyst with the tools necessary to process the tapes from both the EA-6A and EA-6B. When dealing with EA-6A tapes, the analyst must be able to reconstruct the actual flight path of the mission in order to override any false navigational equipment inputs that may render the data useless. Due to the quantity collected by the EA-6A, the analyst was quite capable of correcting any false recordings and eliminating that which is invalid. The requirement for analyst interface in data reduction was in itself justification for additional effort expended in software and hardware development.

Data reduction with the EA-6B presented still another problem, as it was capable of collecting a volume of data that was nearly impossible to reduce via the analyst. In order to speed the processing of this data, software routines were written that filtered out redundant and erroneous data that clutter the tape. Provisions were also included to provide for selected processing, whereby the

analyst selected those emitters he wished to process first.

Within TERPES Software there exists an executive module that was the controlling force of processing within the guidelines of TERPES. It was further subsetted to contain the operating system, peripheral handlers, core management routines, mathematical packages and a set of provisions that allow a degree of degraded mode operations. The implemented operating system was tailored after the CMS-2Q monitor in order to optimize the functions and procedures of TERPES. Whenever possible the OS was written in CMS-2Q with required assembly language routines written in SYCCL. This move to CMS-2 was aimed at conforming to the Navy's concept of a standardized tactical computer language. It also enabled the developers to utilize the software debugging tools presently available in CMS-2. The OS was a set of subroutines that maintained system status, file status, utility programs and provided the timing sequences required to supervise the operations of the system.

The Intercept Module was expanded to allow the system to translate the data received from the aircraft into a reducible format while filtering out that data which is unreliable. The filtering task was done by checking incoming tapes for recorder errors, building format files of intercepted signals, correcting for spurious navigational inputs, reducing the data size by eliminating redundant data, and providing edit routines that permit analyst intervention when required. Also residing in this module were the analog merge routines and the location algorithm. The merge routine permitted the input of data from the analog tapes that will assist in emitter location and recognition. The location algorithm was utilized in the location of emitter sites.

The final module was the File Management Module. This

particular segment contained the interactive software that linked the CP-808 and the Motorola Totalscope. The interface and system utilities were written in CMS-2Q while internal programming of the Totalscope was done in ARC-16 assembly language. The File Management Module was designed to allow the use of an extensive database of emitter information. The NIPS III database of emitter parameters was the basis of this information. The ability to sort and edit returned data also resided in this module.

As designed, the operating system and its transient service routines were placed in the first 10,240 core memory locations. The remaining core locations were available for the loading of software packages that perform mission processing, mission briefing and any other provided system utility. [1]

III. MILITARIZED VS COMMERCIALIZED SYSTEMS

A. PURPOSE

The purpose of this section is to compare by cost, reliability, and general practical considerations the differences between a "militarized" mini-computer which meets military specifications, and a commercial mini-computer which does not meet military specifications. For clarity, "militarized" means conforming to military specifications and "commercial" means not conforming to military specifications.

B. SELECTION

The mini-computer systems selected for comparison were selected on their ability to meet the requirements of TEPPES. Three different computer manufacturers were involved: Data General Corporation manufacturing mini-computers to meet the needs of commercial user; ROLM Corporation manufacturing "militarized" mini-computers using the same circuit design and software as the Data General Corporation mini-computers but with hardware designed and manufactured in accordance with applicable military specifications (MIL-E-16400G and MIL-E-54000) for use aboard ships and in aircraft; and Sperry Univac Corporation like ROLM, manufacturing "militarized" mini-computers. The following specific systems will be compared:

DATA GENERAL

* MODEL 830
* MODEL 1210

ROLM

* MODEL 1602 AN/UYK-19(V)
* MODEL 1664 AN/UYK-28(V)

SPERRY UNIVAC

* AN/UYK-20(V)

C. BACKGROUND

Standard military specifications have been developed to meet requirements in protecting electrical military equipment. One such specification, MIL-E-16400G(NAVY), states:

> "This specification covers the general requirements applicable to the design and construction of electronic, interior communication and navigation equipment intended for naval ship or shore applications. This specification defines the environmental conditions within which equipment must operate satisfactorily and reliably; the process for selection and application of general material and parts; and the means by which equipment as a whole will be tested to determine whether it is acceptable to the navy ... unless otherwise specifically stated in the individual equipment specification, the requirements of this specification (MIL-E-16400G (NAVY)) and any and all specifications cited herein shall apply when this specification is invoked". [14]

D. SYSTEM DESCRIPTIONS

The system desciption and price information for ROLM's 1602 and 1664 and Data General's 1210 and 830 computers was obtained from technical descriptions and price lists furnished by the manufacturer. The Sperry Univac system

description concerning the AN/UYK-20(V) was also obtained from technical descriptions furnished by the manufacturer but pricing information was obtained from NAVELEX Washington D. C. (AN/UYK-20(V) F/Y 76 Budgetary Estimates). Using this technical and price information a basic system configuration was compared to determine differences in each system.

The basic computer system for comparison purposes consisted of 32K core memory, a central processor, a control panel, a power monitor, and an automatic restart capability. A floating point processor was considered a major factor. The only computer not offering a floating point processor was Data General's Model 1210. Each system is described briefly below.

1. FCLM Corporation

a. Model 1602

The Model 1602 was a 16 bit general purpose "militarized" computer with an optional floating point processor, conductive cooling to the case, memory increments in 8K increments, and two versions of control panels, one physically bolted to the main frame and the other connected by cable. [16]

b. Model 1664

The Model 1664 is also a "militarized" computer but with greater capability than the Model 1602 due to bit addressing not limited to conventional word boundries, variable addressing modes, conductive cooling to the case

with a chassis mounted heat exchanger, standard floating point processor, direct memory access processor, three degrees of precision, and memory increments in 16K bytes increments. [9,15]

2. Data General

a. Model 830

The Model 830 was a non-militarized computer with memory expansion up to 256K, 16 bit instructions, high density core memory, an optional floating point processor, and dual operation through two central processor boards. [23]

b. Model 1210

The Model 1210 was a scaled down version of the Model 830 with a slower memory cycle time, no floating point option and slower arithmetic execution times. [22]

3. Sperry Univac

a. AN/UYK-20(V)

The AN/UYK-20(V) was a "militarized" computer with 16 bit instructions, direct access to a maximum of 65K words, memory increments in 8K increments, a maximum of 65K words of core memory, an optional floating point capacity, self contained internal cooling system, and modular construction. [10]

See Table 1 for an overall comparative view of each computer system. [10,15,16,26]

	B 02	1664	830	1210	UYK-20
Militarized.	yes	yes	no	no	yes
Memory Cycle Time..	1usec	1usec	1usec	1.2usec	750nsec
Memory Direct Addressing.	64K	128K	64K	32K	65K
Maximum....	256K	512K	256K	64K	65K
Transfer Rate....	1M words /sec	1M words /sec	833K words/sec	833K words/sec	1M words /sec
Software Support...	Fortran Algol Basic	Fortran Algol Basic	Fortran Basic	Fortran Basic	Fortran Ultra 16 CMS-2M
Word Size...	16 bit	16 bit	16 bit	16 bit	16 bit
Power Fault/ Auto-Restart....	yes	yes	yes	yes	yes
Cooling.....	con-ductive	con-ductive	none	none	internal blower
Floating Point.....	yes	yes	yes	no	yes
Ownership Costs.....	$62873.		$23897.	$11357.	$40805.

TABLE 1

Ownership costs included initial purchase price and maintenance costs which were discounted at 6% over a five year period.

See Appendix C for detailed descriptions of each computer system.

4. Price Data

Using the price information provided by the manufacturers and NAVELEX Washington D. C. comparative prices for the selected configurations were determined as follows:

a. Eclm Corporation

(1) Model 1602

Processor unit with 5 MHZ microprocessor, four accumulators, direct memory access, multimode priority interrupt system and a power monitor with automatic restart	...$12750
rugged control panel	... 2500
floating point	... 300
external memory chassis (16K)	... 4000
external memory control	... 1000
external memory port	... 2000
memory chassis (24K)	... 2000
memory interface	... 100
core memory(8K) at $6000 * 4	... 24000
total	$48,650

[17]

(2) Model 1664

Processor unit with 5MHZ microprocessor variable precision floating point processor, direct memory access, executive mode, 16 levels of programmable priority interrupt with power monitor and automatic restart ...$24950
rugged control panel ... 3125
core memory (16K) at $6250 * 2 ... 12500
total $40,575
[17]

b. Sperry Univac Corporation

(1) AN/UYK-20(V)

Basic machine with 8K core memory ...$21000
8K core memory modules at $1300 * 3 ... 3900
direct memory access, factory installed... 2850
math pac, factory installed ... 2100
includes floating point
total $29,250
[19]

c. Data General Corporation

(1) Model 830

Computer with four accumulators (hardware), I/O system with programmed data transfer 16 level programmed priority interrupt, direct memory access data channel, programmer's console with lock, power supply and slide mounts for a 19 inch rack, 32K bytes core memory and memory management and protection unit. ...$12650

power monitor and automatic restart ... 400

multiply/divide ... 1000

floating point unit ... 4000

total $18,050

[18]

(2) Model 1210

Computer with four accumulators (hardware), I/O system with programmed data transfer, 16 level programmed priority interrupt, direct memory access data channel, programmers console with lock, power supply, table top cabinet or slide mounts for 19 inch rack, and 32K bytes core memory. ... $7000

power monitor and automatic restart ... 400

multiply/divide ... 1600

total $9000

[18]

Appendix B gives a breakdown of pricing information for each system.

E. RELIABILITY

Up to this point, this chapter has dealt strictly with system description and the associated costs. If cost were the only criterion for selection, Data General would be chosen without question. But cost should not be the only criterion; reliability of the system should be a major consideration in the decision. By evaluating the reliability of a computer system using Mean Time Between Failure (MTBF) and repairability using Mean Time To Repair (MTTR), the cost of ownership beyond the initial purchase price can be estimated.

Because there was no data on MTBF and MTTR for the ROLM Model 1664, this computer system was not considered in the reliability analysis.

The data that was available was supplied by ROLM Corporation, Data General Corporation, and the General Electric Company in an article titled "MAGIS LIFE CYCLE COST ANALYSIS for the Marine Air/Ground Intelligence System".

One way to estimate failure rate is through reliability experience. As outlined in MIL-STD-756A and MIL Handbook 217A/B, there are standard procedures for estimating failure rates given component types and part numbers. For the purposes of this study, the computer systems involved were in actual operation. However, the standards as stated in MIL-STD-756A and MIL Handbook 217A/B were followed where necessary.

Failure rates are normally considered large initially during burn in of components, then decreasing to remain relatively constant for some time. This reflects equipment failure under the assumption that new equipment has frequent

repairs after which a stable period is established. This stability period is characterized by random failures. Wear out does not occur in electrical equipment as it does in mechanical equipment. However, due to extensive bench testing and modular integrated construction, the failure rate of new equipment has been reduced (compared with systems that are not extensively bench tested). Consequently, after the initial burn in, the failure rate of computer equipment is constant with respect to time. Therefore, the number of failures can be estimated by the Poisson distribution and the time between failures by the Exponential distribution. The probability of zero failures in time t (reliability) is given by the equation:

$$P = E^{-lambda * t}$$

where LAMBDA is the failure rate or 1/MTBF.

This evaluation will assume that once a failure has occurred, the repair will be made at the module level, not the component level, and that time for a repairman to arrive at the computer site for repair work will be two hours. The Mean Time To Repair, once a repairman arrives, was assumed to be one-half hour for all computer systems. This was the mean time required to find the failed module, remove it, and replace it with a new one. The reason all MTTR's were assumed equal was based on the modular construction used in all the computer systems. The difficulty of board removal was approximately the same for all systems.

For the purpose of this evaluation, the cost of ownership over time t (5 years) was based on purchase price, inventory cost of spare kits, and repair cost. Inventory cost and repair cost were discounted at a 6 percent rate for

5 years to reflect the time value of money. The discount factor was .747. Based on the equal MTTR's for each computer system, only the MTBF was found to affect the final cost of ownership.

Inventory cost consisted of the cost of the minimum spares necessary to repair a failure. A minimum spare kit consisted of one spare memory module, one processor module, and one power supply module. [20]

Repair costs were calculated by multiplying the mean number of failures during time t (t/MTBF) by the MTTR and then multiplying this result (or the average amount of time spent on repair during time t) by the labor rate per hour. For clarification, the following symbols were defined:

T : useful lifetime of the system (5 years)
MTBF : mean time between failure
MTTR : mean time to repair
(including time for repairman to arrive)
I/MTBF : number of failures in time T
TR : (T/MTBF) * MTTR
(average time spent on repair during time T)
SM : spare kit cost (based on minimum kit needed)
RCH : repair cost per hour
ATR : RCH * TR (average cost of time spent on repair)
IRC : ATR + SM (inventory and repair cost over 5 years)
TVC : time value cost (IRC with time value of money
taken into consideration at 6 percent)
OC : ownership cost (TVC + initial purchase price)

Table 2 contains specific calculations of each system.

	1602	830	1210	UYK-20
MTBF	13200 hrs	4510 hrs	6718 hrs	2000 hrs
MTTR	2.5 hrs	2.5 hrs	2.5 hrs	2.5 hrs
I/MTBF	3.23 hrs	9.47 hrs	6.35 hrs	21.36 hrs
TR	8.07 hrs	23.67 hrs	15.87 hrs	53.4 hrs
SM	$18750	$7000	$2600	$13600
RCH	$36	$35	$35	$35
ATR	$290.52	$828.45	$555.45	$1869.00
IRC	$19040.52	$7828.45	$3155.45	$15469.00
TVC	$14223.27	$5847.85	$2357.12	$11555.00
OC	$62873.27	$23897.85	$11357.12	$40805.00
	[17]	[18]	[18]	[19]

TABLE 2

Excluded from the cost of repair were those items that contributed equal cost to all the computer systems. These items consisted of travel cost, per diem cost, and shop

repair cost (cost of repairing the failed module, in the manufacturer's shop). [21,22,23,27,28,32]

Table 2 shows that the Data General 1210 cost less over 5 years based on inventory cost, repair cost, and the initial purchase price of the computer (purchase prices were taken from section 4 "Militarized vs Commercialized"). Referring to Table 2, the high cost of ownership does not reflect high MTBF as might be expected. The Sperry Univac AN/UYK-20(V) had the second highest ownership cost but the lowest MTBF.

Figure 1 is a plot of the relationship between MTBF and the total cost of ownership. While there is no direct relationship between MTBF and total cost of ownership, Figure 1 indicates, at the low point of the "U" on the curve, that the Data General Model 1210 would be the logical choice with the lowest ownership cost and the second highest MTBF. The difference between the Data General Model 1210 and the RCLM Model 1602, as reflected in Figure 1, would be a doubling in the MTBF but a five fold increase in cost. Specifically, to get a 6482 hour increase in the MTBF, it would cost $51516.09 over a 5 year period.

Figure 2 represents the relationship that existed between the MTBF and the cost of repair over a 5 year period. Referring to Figure 2, as MTBF goes up the repair cost goes down. For example, if the MTBF went up from 4000 to 8000 hours there would be a corresponding $450 savings on repair costs.

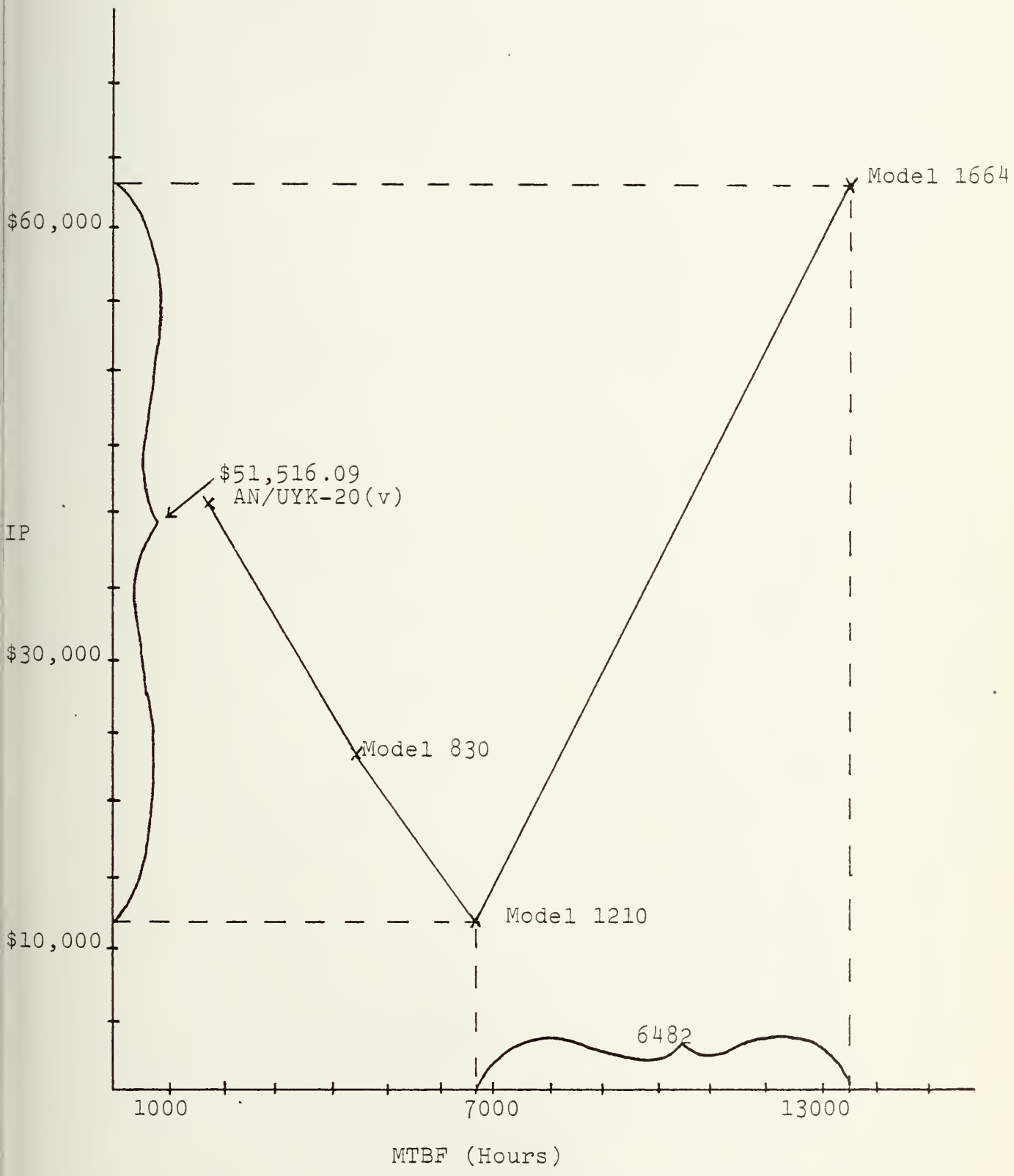

Figure 1 - MTBF vs TOTAL OWNERSHIP COST

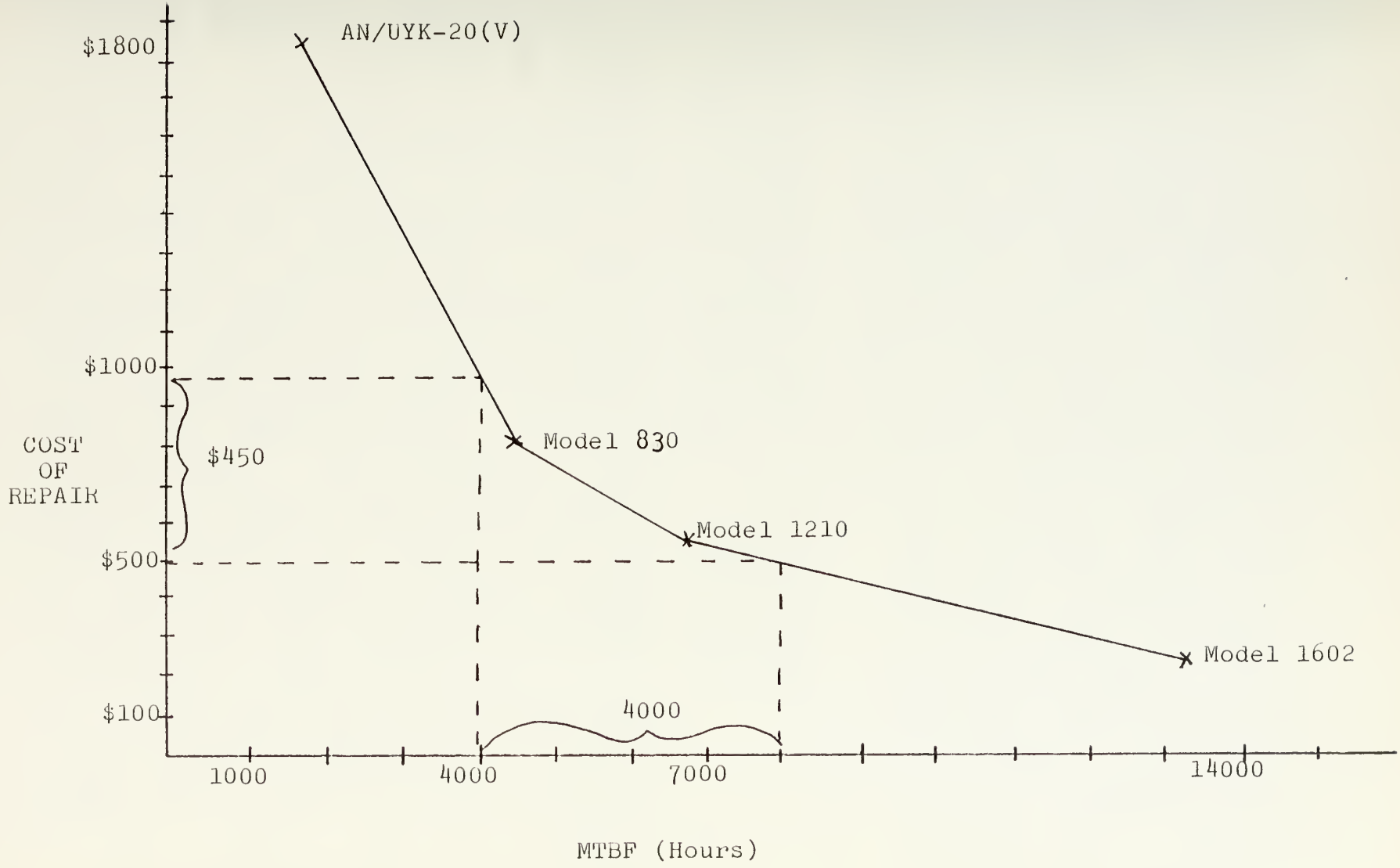

Figure 2 - MTBF vs COST OF REPAIR

The wide variation between the MTBF's (one major failure every 550 days for the ROLM Model 1602 compared to one major failure every 83 days for the Sperry Univac AN/UYK-20(V), seems unrealistic since the difference is between two militarized computers. The MTBF of the Model 1602 was furnished by the ROLM Corporation seems too high. The MTBF for the Sperry Univac AN/UYK-20(V) does not seem unreasonable. This MTBF was not furnished by Sperry Univac but by a military analysis group. [21] The following MTBF's are the values necessary to make a systems spares cost equal to the ROLM Model 1602 spares cost.

Data General Model 1210 ..... 320 hours
Data General Model 830 ..... 235 hours
Sperry Univac AN/UYK-20(V) .... 700 hours

Militarized and commercialized computer systems each have advantages. If a commercialized computer is acceptable in the operational environment, then there are numerous systems available that are comparable in both cost and performance. With respect to TERPES requirements, the Data General Model 830 had a capability advantage over the Data General Model 1210, the advantage being the availability of a floating point option. Otherwise, the Data General Model 1210 was superior in purchase price, cost of ownership, and spare kit cost (see Table 2). The difference between the MTBF's of the Data General Model 830 and the Data General Model 1210 was one failure every 108 days in favor of the Data General Model 1210. While this failure difference was significant, the lack of overall capability of the Data General Model 1210 compared to the Data General Model 830 should be a major consideration, regardless of the MTBF's.

Although there is no published MTBF for the ROLM Model 1664, this should not eliminate it from the competition. The ROLM Model 1664 contained a Tri-Processor System (hardware floating point processor, a microprogrammed general purpose processor and a direct memory access processor) versus one general purpose processor for the ROLM Model 1602, costs less than the ROLM Model 1602 to purchase, and is capable of expansion for future considerations. Regardless of the MTBF, the spares kit for the ROLM Model 1664 would cost $6500 more than the spares kit for the ROLM Model 1602 or $24,750 in total. The ownership cost of the ROLM Model 1664 over a 5 year period could never be equal to the ROLM Model 1602, regardless of the MTBF, since the initial spares kit cost of the ROLM Model 1664 was more than the ownership cost of the ROLM Model 1602. Although the Sperry Univac AN/UYK-20(V) had the lowest published MTBF, the figure seems conservative. The MTBF should not be the major reason for eliminating it from the competition.The Sperry Univac AN/UYK-20(V)'s cost of ownership was less than the ROLM Model 1602 (due to spare kit cost) and had a $19,400 advantage on purchase price over the ROLM Model 1602.

One important factor, which would be difficult to measure in dollar terms and not represented is the cost to the mission of down time. This cost, which could conceivably involve thousands of dollars, includes such items as down time of planes, travel and berthing of personnel if the mission were cancelled. Because of this factor, a high MTBF becomes a very critical consideration.

IV. PERFORMANCE REQUIREMENTS

A. INSTRUCTION RATINGS

One measure of performance that must be addressed in any processor replacement proposal is the question of processing power. By performing such an analysis the steering committee must attempt to demonstrate in a quantitative manner that the processors under consideration are capable of handling the processing load that exists on the older machine.

It was determined that the first step in this type of analysis was to describe an instruction mix that would reflect the construction of programs within TERPES. Although the software was being developed, it was possible to estimate the mix and assign the following percentages:

INSTRUCTION TYPE	% of USE
Set/Clear	15
Compare	15
Shift	15
Transfer	15
Load	10
Store	10
Arithmetic	10
Logical	10
Total	100

Utilizing the instruction mix anticipated within TERPES,

it was estimated that the CP-808 average instruction execution speed was 8.7 usec. yielding an instruction rate of 115K instructions/sec.

At this point a problem was encountered with word length. As noted in a previous section the CP-808 operates with a 30 bit word, whereas, proposed replacement minicomputers operate with a 16 bit word. To overcome the word length inequity, an instruction rate for double word instructions (32 bits) and single word instructions (16 bit) were computed seperately. Another consideration was to utilize, wherever possible, instructions that access memory directly. [7]

The Sperry Univac AN/UYK-20(V) was found to have an average instruction time for double word instructions of 2.84 usec. with an instruction rate of 352K instructions/sec. The single word average instruction time for the Sperry Univac AN/UYK-20(V) was found to be 2.27 usec. with an instruction rate of 440K instructions/sec. [10]

Due to the similarity of execution times between the Data General machines and the ROLM computers, it was decided that one set of computations would be sufficient to demonstrate their processing power. Using double word instructions the average instruction time for this class of machine was 3.45 usec. or 290K instructions/sec. Single word instructions were processed with a time of 2.755 usec. or an instruction rate of 362K instructions/sec. [9,11]

As shown above the machines under consideration could easily handle the processing load being performed by the CP-808. This excess processing power is essential if the full potential of TERPES is to be ever realized in the area of real-time operation and mission planning.

B. ARITHMETIC PRECISION

Having demonstrated the processing power of the proposed replacement processors, it was necessary to examine the precision they offered in arithmetic calculations. The importance of this attribute lies in the primary mission of TERPES, which was the identification and location of hostile emitters. In order to ascertain the location of a particular emitter, the direction of arrival data extracted from the mission tape was applied to a locator module that contained the location algorithm. It was in this section that arithmetic precision became critical, for if a number of significant bits of data were lost in the calculations, the chances of producing a reliable site plot were minimal.

The CP-808 hardware normally provided fixed-point computational data elements which occupied a maximum of 30-bits (one word). Another feature of the CP-808 was the ability to link the A register and the Q register to form a double-length word that supported data elements that were 60-bits in length. The A register was a 30-bit addressable accumulator, while the Q register was a 30-bit addressable logical function register. This double-length feature was employed in the emitter location algorithm as a software feature to extend the precision of arithmetic calculations.

This 60-bit fixed point double precision feature was an option that was not available on any of the processors under consideration. At this point it was determined that there were only two options available to overcome this problem. The first involved determining the precision that would be needed to satisfy the requirements of TERPES. The first step in such an analysis was to determine the accuracy of

the data returned by the aircraft. The emphasis at this point was to ascertain the number of bits that contained reliable location data for a given emitter. With this information it would have been possible to calculate the number of bits of significance required to maintain the specified precision when computing an emitter's location. During the developing stages of this analysis, it was determined that the required data needed to perform such an analysis was not available.

This lack of data led to the second approach, which was to examine the way the proposed processors represented numerical quantities internally. It was decided that the representation that would most likely solve the precision problem would be a floating point representation.

In this set of calculations, precision was taken to mean the number of bits available to represent a number. The number of decimal-digits of precision was compared. For these calculations n was taken to be the binary bits of precision and m was the number of decimal digits of precision. It was then necessary to solve for m in the following:

$$10^{m} = 2^{n}$$

$$m \log_{10} 10 = n \log_{10} 2$$

$$m = n(0.30103) \qquad [8]$$

The results of these computations are represented in the following table:

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$$10^{m} = 2^{n}$$

$$m \log_{10} 10 = n \log_{10} 2$$

$$m = n(0.30103)$$

[8]

The results of these computations are represented in the following table:

DECIMAL-DIGITS of PRECISION

- CP-808
  - Single Precision 9
  - Double Precision ..... 18 [2]
- ROLM Model 1664 (Floating Point Processor)
  - Single Precision
    - 32-bit format 7
  - Extended Precision
    - 48-bit format 12
  - Double Precision
    - 64-bit format ..... 16 [9]
- Sperry Univac AN/UYK-20(V)
  - 32-bit format ..... 7 [10]

As noted in the above table, the location algorithm, when executing on the CP-808, was operating with 18 decimal-digits of precision. It was estimated that such precision was excessive, but a 32-bit format that yielded 7 decimal-digits of precision was insufficient. Having demonstrated the precision available within the various hardware configurations the only competitor that approached the precision of the current system was the Floating Point Processor available from both ROLM and Data General. In the ROLM machines it was implemented as an integrated processor that paralleled the general-purpose processor. The Floating Point Processor consisted of eight 64-bit accumulators and one 32-bit status register that were addressable by a set of 51 Floating Point Processor Instructions. Operations between memory and the FPP accumulators were also fully supported.

In conclusion, it was determined that a complete analysis of the accuracy of returned data was essential to insure adequate arithmetic precision. With the above analysis completed it would then be possible to adequately evaluate the various machines to determine if the required precision can be obtained through software, firmware, or a hardware device.

V. SYSTEM ACQUISITION

A. PROCUREMENT

The "Code of Federal Regulations 41" and "Federal property Management Regulations, Part 101-32, Government-wide Automated Data Management Services" specifies requirements concerning the acquisition of data processing equipment. The primary requirements cover sharing activities, commercial acquisition, sole source restrictions, use of existing federal contracts, competitive bidding, and standardization and interchangeability of parts. These requirements, as presented below, are not exhaustive and should only be considered as highlights to the overall process of procuring a new data processing system.

1. Sharing Facilities

The first consideration, as viewed by the Federal Government, is whether or not the proposed system could be supported by "sharing" facilities with an existing system, government or commercial. Automatic Data Processing (ADP) sharing means the use of available ADP resources by organizations that the organization providing the resource does not have a primary mission responsibility to support. The Federal Agency requesting the proposed system cannot initiate the process of selecting and acquiring ADP time or services from commercial sources unless it has first

determined that the required ADP capability cannot be met satisfactorily by utilizing existing Federal ADP resources or established Government Services Administration (GSA) mandatory contractual resources. Based on the objectives of the TERPES system and the uniqueness of the requirements, the possibility of utilizing a "sharing" facility is not a viable alternative in selecting a new system.

2. Requirement Type Contracts

The next consideration in procuring ADP equipment (ADPE) is through requirement type contracts. GSA makes selected ADPE available to agencies through requirement type contracts when such contracts will provide for substantially lower equipment cost. Where ADPE is available from GSA requirements type contracts, this source shall be used by all agencies as the primary source to satisfy needs in accordance with the provisions of such contracts. If this type of contract is not used, agencies may procure ADPE without prior GSA approval provided (1) the procurement will occur through an applicable ADP Schedule contract, (2) the contract is with a company that already has a Schedule contract but the requirements of the new procurement are unable to be carried on the original Schedule contract. Consequently, a new contract is written with terms equal or better than the terms in the original Schedule contract. (3) the value does not exceed $50000.

3. Sole Source

Sole source procurement of ADPE in excess of $50000 over the systems life by either lease or purchase is permitted only after a delegation of procurement authority (DPA) is provided by GSA. Where a sole source procurement

appears to be in the best interest of the Government, agencies must submit to GSA a request for a DPA along with a statement justifying the requested action. The determination must be accompanied by a certification of the availability of specifications in accordance with the provisions of GSA directives. After review of the APR and any other documentation essential to the justification, the Commissioner, Automated Data and Telecommunications Service will (1) grant authority to the requesting agency for procurement, (2) grant authority to the requesting agency for procurement and provide for participation in the procurement, (3) provide for procurement by GSA. Interestingly, if no action is taken by GSA within 20 working days after receipt of full information from the requesting agency, the agency may proceed with procurement as if approval had been granted. However, the day of receipt of full information, as viewed by GSA, is a debatable date. "In order to establish a common understanding of the 20 working day period, GSA will provide written verification to the requesting agency which identifies the day of receipt of an APR. This day is subject to written modification by GSA in the event that after review it was found that the APR does not contain the full information required...". [24,25]

4. Mixed Installations

While there are restrictions on sole source suppliers, there are major factors to be considered in a multiple source installation.

There are definite dollar savings in procuring or leasing peripheral or main frame equipment from 2nd or 3rd parties. For instance there is an approximate savings from 20 to 25 percent on tape drives, 20 to 25 percent on disk

drives, and up to 50 percent on memory. In addition to these savings, there are benefits such as no overtime cost, quantity price discounts, and 10 to 30 percent savings on 3rd party maintenance. Processors may also be obtained with a relative savings compared to the existing system from 3rd party renting companies. [46]

Besides the obvious dollar savings, there are other factors to be considered in the decision as listed below: (1) installation ADP budget (2) security considerations (3) geographic location of maintenance support for the new equipment (4) delivery time and installation and conversion time needed for the new equipment (5) contractor flexibility with regard to time periods required to achieve lower lease rates (6) time of next conversion; a new contract could lock the installation into using the same equipment for several years (7) supplier staying power (is the supplier established?) (8) split maintenance responsibility; this could be the biggest problem because the lines of maintenance responsibility; this could be the biggest problem because the maintenance responsibility for failed equipment would be difficult to delineate.

Beyond the considerations listed above, there are hidden factors that must be discussed and utilized before any decision is made. First, the fear of unreliable operation if the system is changed. Second, performance improvements might not materialize as planned if the system is changed. And third, if a long term lease is required to obtain the cost savings, the flexibility of the system operation could diminish. This could be disasterous to the user.

5. Competitive Bidding

The aspect of a sole source supplier naturally leads to the requirements of competive bidding. Item 1-3.210 of the Code of Federal Regulations discusses the impracticability of securing competition by formal bidding. Briefly, this states that purchases and contracts may be negotiated without formal advertising "for property (ADPE) or services for which it is impracticable to secure competition."[24] To use this authority the circumstance must exist that the property or service can be obtained from one person or firm (sole source of supply) . ADPE is technical equipment which could require standardization and interchangeability of parts. Based on this fact ADPE contracts can again be negotiated without formal advertising according to 1-3.213 in the Code of Federal Regulations. Application to this item falls within the specification stating "where in special situations or particular locaties, technical equipment is available from a number of suppliers which would have such varying performance characteristics (not withstanding detailed specifications and rigid inspections) as would prevent standardization and interchangeability of parts. Basic to all of these specific considerations is the underlying requirement that all purchases and contracts, whether by advertising or by negotiation, shall be made on a competitive basis to the maximum practical extent. [24]

B. FUNDING

Regardless of the source of the new system for TERPES, funding has to be a major consideration. One solution may be the Automatated Data Processing Fund. This fund is utilized when the purchase evaluation indicates it is in the best interest of the Government to purchase or utilize long term leases and funds are not readily available within the requesting agency or there is insufficient time to secure the necessary funds under normal budgetary procedures, including reprogramming the required funds. GSA will make the determination whether or not the funds will be used. If GSA determines to use the ADP funds, GSA will carry out the acquisition and retain the title to the ADPE with the requesting agency establishing common grounds between itself and GSA for either installment payment or a lump sum payment reimbursing the ADP fund. The requesting agency will, in effect, have a lease with GSA during the payback period which includes equipment cost and authorized personnel services. [24,25]

VI. COMPUTER FAMILY ARCHITECTURE

Before a decision is made for any specific computer system satisfying the needs of TERPES, the project entitled "Computer Family Architecture (CFA)" initiated by the Naval Research Lab (NRL) under the sponsorship of the Naval Air Systems Command in conjunction with the Army Electronics Command should be thoroughly investigated. Due to the nature and impact of this project, the feasibility in waiting for the outcome of this project before deciding on a computer system would be a sensible and rational decision.

The CFA project evolved from the All Application Digital Computer Program seeking to obtain for the Army and Navy a computer architecture which will serve as the basis for a family of software-compatible computers, that can be implemented at various performance levels using advanced technologies. Particularly important is the 1981 time frame when CFA is to be fully implemented. It is recommended that any decision on new equipment be made only after fully considering the benefits to be gained from the CFA approach. Besides the time frame compatability, CFA would do away with the consideration of sole source distribution and any associated problems concerning competitive bidding on contracts.

The specific program goals of CFA include: competitive cost effectiveness for a wide range of Army, Navy, and Marine Corps applications; significant improvement in software/hardware life cycle cost; significant reduction in hardware size, weight, and power; alternative suppliers; technology independent; and 3rd generation software

transportability. More specifically, computer architecture is the functional description of a computer as would be seen by a machine level programmer, that is, everything the programmer needs to know to write programs that run on the computer. This view of the computer includes the instruction set, registers, interrupts, and memory address space. The architecture does not include hardware implementation features such as cycle time, instruction look ahead, memory interleaving, bus width, or cache memory. Hardware design issues need not affect the software. More importantly, a clear and clean distinction between the architecture and implementation details allows software to be transported between computers with the same architecture even though they may have very different features. Standardization of architecture permits the option of choosing different hardware implementations according to the best technology that industry has to offer while maintaining a consistent and well known interface for software developement and education.

The selection criteria for CFA consisted of two parts, absolute criteria and quantitative criteria. Absolute criteria must be fully met. Failure to meet any of the specified absolute criteria means elimination of that particular computer architecture from futher consideration. There are eight absolute criteria including virtual memory support, protection, floating point support, interrupts and traps, modularization, multiprocessor support, controllability of I/O, and extendability. Quantitative criteria will be used to rank those architectures that pass the absolute criteria. Quantitative criteria include virtual address space, physical address space, fraction of instruction space unassigned, size of central processor state, virtual machine capability, maximum interrupt latency, and subroutine linkage. After the list of candidate architectures have been narrowed down to the

"finalist", by means of the absolute criteria and quantitative criteria, test programs will be coded and executed for each surviving candidate, to obtain data related to the efficiency of the architecture. The quantitative criteria posed several problems in the areas of linear ranking of the criteria and normalization of the quantitative measures. Both of these problems were overcome through the use of scaling and composition of quantitative measures, the calculations of which are not pertinent to this paper. However, what is pertinent is that a common measure was established to rank the different architectures on a linear scale.

The CFA committee reduced the number of candidates from nine to four, using the absolute and quantitative criteria. Still left in the competition are the Interdata 8/32, the DEC PDP-11, the IBM 360/370, and the Burroughs 6700. The Sperry Univac AN/UYK-20(V) and AN/UYK-7 were both eliminated under the absolute criteria. Both failed the absolute criteria of protection based on the fact that some process could hang up the processor indefinately and thus cause other processes to hang-up. Besides this, the Sperry Univac AN/UYK-20(V) failed the absolute criteria of virtual memory and the Sperry Univac AN/UYK-7 failed the absolute floating point criteria. On the quantitative composite scale the Sperry Univac AN/UYK-20(V) and the AN UYK-7 ranked eighth and ninth respectively in the field of nine candidates. The Litton GYK-12 (lacked floating point capability), the RCLM 16C2 (lacked virtual memory), and the SEL-32 (lacked virtual memory) also failed as possible candidates.

The current results of the CFA committee should not be interpreted as meaning that the Sperry Univac AN/UYK-20(V) and the RCIM 1602 cannot meet the requirements of TERPES. However, the value of the CFA findings should not be taken lightly, but should be viewed with interest as a planning tool for the future. [29]

VII. PERIPHERAL ALTERNATIVES

One aspect that was initially proposed was a review of the available militarized peripherals. This proposed review would have culminated in a recommended set of state-of-the-art peripherals to replace the present set. While researching this question it was learned that a decision had been made to utilize a commercial disk in the hardware suit of TERPES.

The Disk Storage Unit that was acquired for TERPES was the CDC 9740. This unit was a commercially available device that was not developed or constructed for implementation within the severe environmental constraints of TERPES.

The importance of the disk unit was stressed in the software structuring and development phase because of the expanded capability it provided. With the development phase completed the Disk Storage Unit will have become an essential part of TERPES operations. A failure of this unit would essentially terminate the processing capability of TERPES.

By selecting a commercial disk the credibility of equipment specifications was dealt a damaging blow. At this point it was determined that a review of equipment specifications be conducted by the user community in order to ascertain the reliability and correctness of TERPES equipment specifications. With a user analysis completed, it may be advisable to procure commercial equipment that is housed in industrial enclosures, whereby equipment costs are reduced while the available equipment market expands.

A. PLOTTERS

The purpose of the Calcomp 563 plotter was to provide a hard copy of graphics terminal displays. While plotting comprised about 50% of mission tape analysis time, the plotting cycle was not considered essential to the success of a mission. [1]

1. Militarized vs Commercialized

A militarized plotter would cost approximately $100,000 to buy. The Calcomp 563 costs approximately $6500 to buy or $300 per month to rent. Based on the high cost of a militarized plotter and because the plotter is not mission essential to TERPES, it was felt that there was no need for a militarized plotter. Based on this conclusion, this section will discuss the characteristics of commercial plotters.

2. Types

There were three types of available plotters: flatbed, drum, and electrostatic. The flatbed plotter utilized a flat sheet of paper, held in place, while the writing instrument was moved in two directions to draw lines. The advantage of the flatbed plotter was that additions could be made to existing plots. The disadvantage could be extra space requirements of the plotter, which was dependent on the size of the paper. The drum plotter moved the paper and the writing instrument to produce the lines. The advantage of this unit was that long drawings could be

accomplished in a compact space. However, there were width constraints, which limited the size of the drawings. Electrostatic plotters moved the paper to produce one of the movements and utilized a row of stylii across the width of the paper producing images consisting of a multiple of points. The advantage of this plotter was the speed and the ability to double as a line printer when equiped with a character gernerater. However, the plotting required an unusual programming method for generating line by line point rasters.

Table 3 contains state-of-the-art characteristics for flatbed, drum, and electrostatic type plotters. For comparison, the characteristics of the Calcomp 563 drum plotter are underlined in Table 3. The following characteristic definitions may be useful.

accuracy : pen positioning error
resolution : measure of closeness in drawing lines.
repeatability : measure of capacity of the device to return to a previously plotted point.

	FLATBED	DRUM	ELECTROSTATIC
accuracy	.004 in.	.0025 in. n/a	.01 in.
resolution	.0001 in.	.002 in. .00 in.	200 points/in.
repeatability	.004 in.	.002 in. n/a	n/a
paper movement speed	n/a	30 in./sec 2 in./sec	7 in./sec
pen movement speed	100 in./sec	30 in./sec 2 in./sec	n/a

[37]

TABLE 3

Since the plotting of a mission required 50 percent of the total time to process a mission and because the Calcomp 563 was considered a slow plotter, see Table 3, a faster plotter would be a definite advantage and justifiable from the standpoint of time and speed of plotting. However, faster plotting speeds correspondingly carry higher cost. Therefore the decision on how fast a plotter would be necessary, would depend on the availability of funds.

VIII. PROCESSOR ALTERNATIVES

A. CORE MEMORY EXPANSION

The main thrust of this proposal was to increase the size of main memory in order to support a more complex software structure. The increased memory would have enhanced system throughput by reducing the number of data transfers from peripheral storage.

The first step in this analysis was to determine the possibility of expanding the CP-808's 32K of core memory. The NTDS Advanced Data Management program was confronted with a problem similar to the one facing the TERPES development team. As requirements for information have expanded within the NTDS community the developers were faced with either the purchase of new systems or expansion of the existing systems. The design and implementation of new systems was an endeavor that was constrained by the lack of funds. It was felt that system software life cycle costs would be adversely affected by the proliferation of system configurations which might result from non-uniform integration designs. The proliferation of application oriented systems would increase the cost of equipment maintenance, interfacing, personnel training, and software development/maintenance. In order to maintain the integrity of the extensive software base, it was determined that system expansion was the only viable solution. The implementation of this solution was realized by the development of a distributed processing system which

utilized the CP-642B processors and an extended memory unit. [35]

Of interest to the TERPES project was the availability of an operational memory unit that was capable of being interfaced with the CP-808. The applicable extended memory unit was designed and developed by NELC, San Diego with the commercial contract for equipment construction awarded to the Control Data Corporation.

The designation of this unit was the CDC MU-602(V)/UYK Extended Core Memory Unit. The underlying goal of this device was to offer militarized, high speed core memory to enhance the capabilities of current computer systems. The ECMU had the capability of serving four CP-642B's on a first-in, first-out basis. The interface that was developed between the ECMU and the host computer provided for a direct access of up to a maximum of 294K words of core memory, 32K of which the CP-642B had internally mounted with the remaining 262K words housed in the ECMU. The ECMU was fully militarized and was available in a water cooled or air cooled version. The operational characteristics of the ECMU were;

MEMORY
  Storage Capacity ..... 262,144 36 bit words
  Modularity ..... available in increments of 32,768 words.
  Cycle Time ..... 1.05usec.
SIZE ..... 29 cubic ft.
HEIGHT ..... 72 inches
WEIGHT ..... 1400 pounds
POWER REQUIREMENTS ..... 115 VAC; 3-Phase; 400-Hz; 2400 Watts

Operating Temperature ..... 0^{o} to 50^{o} C

Storage Temperature ..... -62^{o} to $+75^{o}$ C

Maximum Humidity ..... 95 percent

[36]

At the time of this writing, the ECMU's were being produced at the CDC plant in St. Paul, Minn., and the production called for the manufacture of 70 units. It was estimated that any new orders would take about 8 to 12 months to fill. The cost of the ECMU with a full complement of memory boards was estimated at $260K with the possibility of a reduced rate, if a substantial order were placed.

In conjunction with the placement of an order for the ECMU, steps would have to be taken to prepare the CP-642B for the interface. The hardware modification of the CP-642B consisted of a modification kit that must be installed by Univac technicians. The modification was available on-site or at a Univac facility and the cost was estimated at $20K.

The degree of core memory expansion was the next problem addressed. An analysis of the time the processor must be idle waiting for the transfer of utility programs from secondary storage was proposed. This analysis required a thorough knowledge of program size, sequence of mission tape analysis and a means of predicting the probability of having the required programs in core. Due to the ongoing software development, the actual physical size of the programs and the probability of having to wait for the program to be loaded from peripheral storage were unavailable at the time of this analysis. It was determined that this type of analysis was essential in order to ascertain the proper mix of core memory and peripheral memory. It was for this reason that an analysis using theoretical parameters was conducted.

The memory management technique used in TERPES development was a segmented overlay approach.

The application programs within TERPES were modelled after a menu driven system, whereby the analyst steps through his analysis by selecting the aspect of processing he desires. This technique enabled the construction of programs in a sequentially structured format, which enhanced the linkage of various subroutines. After a menu selection, an executive module is loaded with its associated overlays into the task area. A review of the core structure was deemed necessary at this point in order to stress the importance of a well developed core map strategy. The core map strategy employed in TERPES follows:

MEMORY LOCATION	APPLICATION
0 thru 128	Linkage Variables
129 thru 400	Resident Services
	Global Variables
401 thru 8192	System Configuration
	Tables
	System Buffers/Tables
	I/O Drivers
	Resident Services
8192 thru 10240	OS Transient Area
10241 thru 28672	Task Area
28673 thru 32768	Manual Utilities/Loaders

The two important aspects of the above table were space allocation for the task area and the OS transient area. The OS transient area was allocated 2048 words of memory for various executive modules that were used to implement the overlay technique. The task area was allocated 18432 words of memory for application programs (Mission Planning, Mission Briefing and Database Utilities) and their

associated data. The segmented program blocks were 919 words in length and were transferred at a rate of 80000 bits/sec/channel from peripheral storage.

The point of contention was the optimum amount of memory to procure. Reference (38) contained a recommended approach for determing the optimum memory size for a particular system. The heart of this scheme was the production of a parachor curve that graphs total available memory against the number of page faults that occured under varying memory sizes. The resulting graph showed that as memory size was increased the number of page faults decreased to a threshold point, after which an increase in available memory produced no dramatic decrease in page faults.

Due to the lack of available data, the preparation of a similar curve for the various application programs used in TERPES was not possible. The importance of such an analysis cannot be overstressed for its results should produce a suitable memory size.

The page size utilized in Reference (38) was 4K bytes. The block size transferred between the CP-808 and its peripheral storage was set at 919 words. The total address space available for application programs was 20K allowing a total load of 21 segements. Extracted samples of page interrupts from Reference (38) yielded the following transfer times:

MEMORY SIZE	TRANSFER TIMES
32K	1766 sec.
48K	846 sec.
64K	446 sec.
96K	151 sec.
128K	93 sec.

The important aspect of the above analysis was to demonstrate the importance of analyzing the software structure, in order to procure the correct amount of core memory. As the complexity of software increases to meet the future requirements of TERPES, overlay time may dramatically reduce available processing time if insufficient memory space were procured. The desire here must be to enhance throughput to permit a more complex software structure.

In conclusion, it was determined that a memory size that exceeded 32K was a requirement. The construction of a parachor type curve was a recommended technique that should be used to enhance the possibility of purchasing the optimum memory size. It was ascertained that this expanded memory should be incorporated into the procurement of a new machine. Expanding the memory of the CP-808 was not considered to be a feasible option. The major limitations were the excessive cost and space required for the ECMU. Space allocation in the system vans was considered a critical point and a factor that eliminates the introduction of the ECMU. It was further determined that an expansion to the full 262K was not economically feasible. An expansion to 64K or 96K was a better alternative but with such an expansion the physical size of the ECMU was still a limiting factor.

B. SPERRY UNIVAC AN/UYK-20(V)

The Sperry Univac AN/UYK-20(V) had definite advantages and disadvantages as an aternative for TERPES.

1. Advantages

The Federal Government signed a contract with Sperry Univac for the manufacture of AN/UYK-20(V)'s. Because of this contract, the AN/UYK-20(V) will have wide spread usage throughout the Navy and Marine Corps with the associated stocking of parts to support the computers. The design objectives of the AN/UYK-20(V) were aimed at military usage and included the usage in tactical data systems. The support of CMS-2 could be a distinct advantage or disadvantage if the military community, as a whole, selects CMS-2 as its standard language to support all tactical computer applications. Due to the Navy's present committment to CMS-2 as its tactical computer language, the availability of a CMS-2 compiler for the AN/UYK-20(V) must be viewed as a favorable system option. The low relative MTBF of the AN/UYK-20(V) was questionable. Taking into consideration the possible bias of the sources of system MTBF, the cost of the AN/UYK-20(V) was not unreasonable and should not be the sole reason for disqualification.

2. Disadvantages

The number of reasons for eliminating the AN/UYK-20(V) from TERPES consideration presently outweigh the reasons for selecting it. Since the AN/UYK-20(V) was a

completely new design with no established computer for solving known problem areas, the AN/UYK-20(V) will probably experience all the common problems, typical of a completely new system and design. Such problems include:

(1) limited software support
(2) developement of software in house
(3) hardware and software bugs
(4) limited user feedback due to the small number of operating applications
(5) not upward compatible with any other computer
(6) limited expansion capability due to the maximum of 65k of core memory

In particular, if TERPES was utilizing the AN/UYK-20(V) and CMS-2 was the supporting language, the compilation would have to be done with another computer because CMS-2 requires four tape drives for compilation and TERPES will use two tape drives.

Another aspect is the renegotiation of the AN/UYK-20(V) contract in July 1976. The new cost to the Navy of the AN/UYK-20(V) could be drastically changed.

C. OTHER MILITARIZED PROCESSORS

The main advantage that ROLM militarized computers had over the Sperry Univac militarized computers was that the design of the ROLM computers were structured around an existing, established, fully operational computer (the Data General computers). Therefore, the ROLM computers had an established software base, interfacing capability, established operating system, and parts support. Because of

these factors, the ROLM computers were upward compatible, in both hardware and software, which was a big advantage in the area of expansion for future needs. In addition to these advantages the core memory in the ROLM computers was expandable far beyound the limitations of the 65K in the Sperry Univac AN/UYK-20(V).

Recently there were other computer manufacturers entering the militarized field. Because of this, the competition in the militarized field will broaden, bringing lower prices, new technology, and increased capability. In particular, the DEC Corporation was in the process of militarizing the PDP-11.

If the operating environment of TERPES required a militarized computer, the ROLM Model 1664 would be the best choice. Disregarding the unpublished MTBF for the ROLM Model 1664, it was the most powerful, cost less than the ROLM Model 1602, and was expandable for future considerations.

Behind all these considerations was the Computer Family Architecture, CFA, idea. This development should be followed closely in the future, to determine if the outcome of the CFA investigation will have a major impact on the system used in support of TERPES.

D. COMMERCIAL PROCESSORS

The option of using a commercial processor along with all commercial equipment to support TERPES was the most attractive of all the options. This recommendation was based on the operating environment of TERPES, as it did not dictate the use of militarized equipment. Therefore,

numerous attractive aternatives in the realm of ccmmercial equipment became available.

The most attractive aspect cf commercial processors was the cost. Figure 1 showed that the best alternative, based cn price and MTBF, was the Data General Model 1210. Although the Data General Model 1210 was ccnsidered inadequate tc meet the entire needs of TERPES, based cn the sccpe of its processing ability, the next best computer was considered tc be the Data General Model 830 which did meet the requirements of TERPES. However, the ccmmercial ccmputers discussed in this paper, represented only a small portion cf the ccmmercial minicomputer market.

With a large field of ccmmercial alternatives tc chcose frcm, advantages such as extensive software, solid parts support, upward compatability, field-prcven hardware and scftware, and ccmpetitive bidding became important pcints in suppcrt cf ccmmercial computers.

The aspect cf lower cost, relative to militarized prccessors, allowed the possibility to invest in a mcre powerful prccessor and thus giving expansicn capabilities.

The hardware configuratien that suppcrted TERPES was a mixed system which ccnsisted of militarized and ccmmercial equipment. In particular, it utilized a commercial disk unit. Since the disk unit was considered the most critical piece cf equipment in a total militarized system, the existance of the ccmmercial disk unit in the TERPES system supported the recommendation for the entire system tc be ccmmercial.

The disadvantage of commercial equipment was in the possible difficulties in obtaining approval for acquisition. This should not be a deterrent as there are specific procedures for purchasing commercial equipment which may not be as easy as purchasing equipment under existing Federal Contracts, but the savings in cost were considered well worth the effort.

IX. FUTURE ENHANCEMENTS

The implementation of TERPES will in fact enhance the capabilities of post-mission tape analysis. The planned changes will provide the operational user community with a tool with which to update and correct flight path data while providing a mechanism for selectively processing mission tapes.

Although the above points were considered to be essential requirements within the framework of TERPES, there still exists a need for a more sophisticated system to provide timely information to the operational commander. The analysis cycle should be carried on in a real-time environment. The areas that will require extensive time and effort were determined to be mission planning and a data-link capability for TERPES.

A. MISSION PLANNING

Within the structure of mission planning, there exists a requirement to ensure that the characteristics of a mission profile, the mode of aircraft employment, and aircraft force levels be readily available for briefing aircrews. In the area of mission planning, TERPES was structured to permit queries of the Naval Intelligence Processing System Electronic Order of Battle to provide mission threat analysis and jammer requirements to counter specified threats. TERPES-provided-data coupled with strike routes and target assignment were the basis for a mission planning

package.

Given the basic capabilities of TERPES the development team will be required to develop a dynamic system. The system must not only provide a static evaluation of a mission profile, it must also have the capability to adapt to a changing EW environment. The changes that must be addressed are threat emitter deployment/mobility, technological advancements, emitter employment and the impact of reduced equipment performance.

In the final analysis, the strength of any mission planning package lies in its ability to perform the following:

1) define enemy radiation doctrine
2) provide accurate and timely emitter location information
3) project aircraft availability and weapons loading
4) assimilate returned reconnaissance data
5) provide strike aircraft flight characteristics
6) project aircraft vulnerability
7) propose aircraft standoff distances
8) propose aircraft routes of flight
9) provide enroute aircraft coordination
10) provide an effective and efficient intelligence reporting system.

[42,43]

B. REAL-TIME ANALYSIS

The strength of any tactical system is the ability to provide timely information to the operational commander. The

current TEREES requirements do not outline any real-time analysis of data as provided by an on-station aircraft. The ability to perform such an analysis can never be overstressed. The information that is provided in this manner can assist in upcoming mission plans while providing new and possible unusual information that may signal a change in enemy radiation doctrine. When this data is linked to a mission planning package, outgoing aircrews can receive information that cannot only contribute to mission success but can prevent the loss of aircraft and lives.

The timeliness of this information might be realized by utilizing an onboard digital computer that was designed to : (1) provide surveillance over a broad range of frequencies in a dense environment; (2) initial identification and evaluation of signals of interest; (3) filter and maintain parameters of interest; (4) associate direction of arrival data with the received emitter signal; (5) provide a means of structuring received/filtered data for transmission to a remote site for further analysis. [44]

Frazer (Ref. 44) proposed a system that linked a series of Instantaneous Frequency Measurement receivers to a special purpose digital computer. The outputs from the IFM's would be filtered and structured into transmission-oriented data sets by the digital computer and data-linked to another computer for detailed classification, analysis, site plotting, threat evaluation and final integration into the mission planning database. As propsed the IFM's would pass emitter data to the digital computer through a common memory storage area.

The Applied Technology Corporation of Sunnyvale, Calif. produced a small high speed special purpose computer that appeared to fit the needs of an onboard processor. The computer designation was the Applied Technology Airborne

Computer (ATAC) and it possessed the following operational characteristics:

WORD SIZE	16 bits
CYCLE TIME	437 nanoseconds (register to register)
DATA TRANSFER	collect/transfer data to seperate devices simultaneously at a rate of 1000K words/sec.
MEMORY	memory pages (4096 words) operate independently and asynchronously to allow mixing of core memory, read only memories (ROM), and random access memories (RAM)
BASIC UNIT	two direct memory access channels, 8K words of memory, and a program timer.
WEIGHT	3 pounds
DIMENSIONS	6in- by 8in- by 2.5in
MILITARY SPECIFICATIONS ...	meets MIL-E-5400 for temp. range -55^{o} C to $+70^{o}$ C as well as specifications for humidity, vibration, shock, EMI and RFI.

[45]

Besides the adaptation to the EW environment, software exists to perform the special applications required. The software support package was designated as the ATAC Programming Support System. There also existed a set of microprogrammed instructions that assisted in the modification of the system structure for additional special applications.

The above proposal provided a means for developing a real-time system that would produce the information the operational commander required. Although the actual development and implementation of a real-time system was considered to be a rather costly venture, the flexibility it would provide the EW community was immeasurable. One approach to the funding problem would be to extract from an ongoing project the technology and hardware that was developed to meet its goals. Investigation revealed the existence of just such a project, the LAMPS DPU project. The goals of this project were to develop a system that extended the electronic sensors of the fleet. The proposed sensor platform was a LAMPS helicopter equipped with a special purpose EW filtering computer and a data-link device to relay the information received to a larger computer aboard ship for further analysis.

Further discussion of this project was not considered to be within the scope of this thesis. The point to be made was that a real-time application of TERPES may in fact be quite feasible. The feasibility of this application lies in the ability of the TERPES steering committee to extract necessary technology from ongoing projects, rather than to initiate a more costly in-house effort.

APPENDIX A

SPECIFICATIONS

		ROLM		DATA GENERAL		SPERRY UNIVAC
		MODEL 1602	MODEL 1664	MODEL 1210	MODEL 830	AN/UYK-20(V)
SIZE						
central processor	height ...	7.62 inches	7.62 inches	5.25 inches	10.5 inches	20.0 inches
	width ...	10.12 inches	13.21 inches	19.0 inches	19.0 inches	19.0 inches
	depth ...	12.56 inches	15.91 inches	19.0 inches	32.0 inches	24.0 inches
control panel	height ...	7.75 inches	7.75 inches			
	width ...	10.25 inches	10.25 inches			
	depth ...	3.9 inches	5935 inches			
operators console				included in cpu	included in cpu	
external memory						
chassis	height ...	7.62 inches	7.62 inches	none	none	none
	width ...	10.12 inches	10.12 inches	none	none	none
	depth ...	7.9 inches	8.4 inches	none	none	none

	ROLM		DATA GENERAL		SPERRY UNIVAC
	MODEL 1602	MODEL 1664	MODEL 1210	MODEL 830	AN/UYK-20(V)
WEIGHT					
Basic unit with					
32K core memory ...	80.6 pounds	85.4 pounds	65.0 pounds	70.0 pounds	220.0 pounds
POWER REQUIREMENTS					
voltage ...	115 vac	115 vac	115 volts 20	115 volts 20	115 or 208 volts
frequency ...	400 HZ	400 HZ	47-63 HZ	47-63 HZ	400 HZ
TEMPERATURE RANGE					
operating ...	0° C to 65° C	0° C to 65° C	0° C to 55° C	0° C to 55° C	0° C to 50° C
storage ...	-65° C to 125° C	-65° C to 125° C	-35° C to 70° C	-35° C to 70° C	-62° C to 75° C
HEAT DISSIPATION					
maximum ...	95 percent	95 percent	90 percent	90 percent	95 percent
condensation present ...	yes	yes	no	no	yes
ALTITUDE					
maximum operating ...	80,000 feet	80,000 feet	10,000 feet	10,000 feet	80,000 feet

	ROLM		DATA GENERAL		SPERRY UNIVAC
	MODEL 1602	MODEL 1664	MODEL 1210	MODEL 830	AN/UYK-20(V)
VIBRATION					
without vibration isolators					
force	3g's	3g's	unknown	unknown	3g's
frequency	5 HZ-1KHZ	5 HZ-1KHZ	unknown	unknown	5 HZ-1KHZ
with vibration isolators					
force	10g's	10g's	unknown	unknown	10g's
frequency	5 HZ-2KHZ	5 HZ-2KHZ	unknown	unknown	5 HZ-2KHZ
SHOCK					
force	15g's	15g's	unknown	unknown	15g's
duration	11 mseconds	11 mseconds	unknown	unknown	11 mseconds
MISCELLANEOUS	sand, dust salt spray, salt fog, fungus resistant [16,37]	sand, dust salt spray, salt fog, fungus resistant [9,15]	unknown [22]	unknown [23]	sand, dust salt spray, salt fog, fungus resistant [10,30]

APPENDIX B

PRICING INFORMATION

	1602	1664	830	1210	AN/UYK-20
Basic Machine	$12750	$24950	$12650	$7000	$21000
Control Panel	2500	3125	n/c	n/c	n/c
Floating Point	300	n/c	4000	n/a	2100
32/K Memory	33100	12500	n/c	n/c	3900
Multiply/Divide	n/c	n/c	1000	1600	n/c
Auto Restart	n/c	n/c	400	400	n/c
Direct Memory	n/c	n/c	n/c	n/c	2850
total	$48,650	$40,575	$18,050	$9000	$29,250

[17,18,19]

APPENDIX C

EQUIPMENT DESCRIPTIONS

A. ROLM CORPORATION

1. Model 1602 Specifications

The Model 1602 (AN/UYK-19(V)) was a 16 bit general purpose "militarized" computer. The microprocessor executed 32 bit micro instructions at a 5 MHZ rate. Twenty five full length registers were available at the microprogram level. One-eighth of the microprogram capacity of 4K words was utilized in implementing the Model 1602 instruction set. The Model 1602 utilized conductive cooling to the case, thus eliminating internal fans or coolants, resulting in a sealed structure for strength and EMI (electromagnetic interference) protection. Hardware multiply/divide, double word instructions, hardware stack instructions, n-bit shifting capability, and a file search were standard. The cpu chassis had room for 8K of 1 microsecond core memory. Memory expansion provided for additional memory, in 8K word increments, to a maximum of 256K. Instruction classes that were standard on the Model 1602 included:

* signed/unsigned, multiply/divide
* file search and compare
* double word memory reference instructions
* additional arithmetic and logical operations

* stack oriented instructions with hardware pointers
* single/double accumulators, n-bit shifts

Optional features included:

* Floating point firmware, providing single precision (24 bit +sign and 7 bit exponent) floating point instructions.

* Semiconductor ram (random access memory) which offers 450 nsec read cycle time memory utilizing a static cmos chip.

* Dual port memory allowing memory in any external memory chassis to be shared by two processors.

* Peripherals include magnetic disk, magnetic tapes, paper tape reader/punch, card readers, line printers, analogue/digital I/O, and NTDS equipment.

The Model 1602 was available in three versions of the ATR (air transportable rack) chassis , two of which contained 8K of core memory with the chassis. The third configuration for systems with more than 32K words of core memory, contained no core memory within the chassis. In all versions additional core memory increments can be attached to the chassis. Each computer chassis contained a power supply, the control processing unit (9 circuit modules), and additional slots for core memory and I/O or memory modules. Core memory increments of 8K words were packaged on four circuit modules which plugged into a computer chassis or one of three memory chassis. The Model 1602 control panel was available in two versions. One is designed to attach to the computer or memory chassis becoming an integral part of the system. The other was designed to connect by cable to the computer. Both had the standard ATR cross section, self

contained power supply, and LED display.

The Model 1602 met military standards MIL-E-16400G class I for shipboard use and MIL-E-5400 for aircraft use. The inspection pro The inspection program on the Model 1602 met MIL-I-45208A class I and the quality assurance procedures met with guidelines of MIL-Q-9858A. [16]

2. Model 1664 Specifications

The Model 1664 had a hardware floating point processor, a microprogrammed general purpose processor, and a direct memory access processor with an executive mode permitting complete memory access and I/O protection.

The Model 1664 used a bit addressing organization that was not limited by conventional word boundaries. Addressing may be by bit, byte, word, field, block, or byte string and list. There are 17 registers of various lengths that are directly available to the programmer. The Model 1664 offered a choice of six addressing modes which consisted of direct, indirect, relative, indexed, base, and auto index. Up to 128K bytes of core memory could have been addressed directly by means of the extended memory reference instructions and any point in memory may be addressed by any other point in memory.

Conductive cooling was employed in the Model 1664 with an additional wrap around chassis mounted heat exchanger which drew air past cooling fins attached to the outside of the chassis.

The floating point processor performed a wide range of floating point arithmetic operations, as well as converting data between integer and floating point format.

The variable precision feature of the processor gave the computer the ability to handle the internal handling of information as well as efficient use of memory space and execution speed.

The direct memory access processor performed direct two way data transfer between memory and any peripheral device at byte rates of up to 2M bytes per second. This processor operated independently of the other two processors.

The multi-accumulator hardware floating point processor was internal to the Model 1664. The standard arithmetic instructions (add, subtract, multiply, divide, fixed and floating point) had been enhanced by the addition of square root, inverse integer, comparison, set status, and test functions. Three degrees of precision were offered in the Model 1664, 32 bit single precision, 48 bit extended precision, and 64 bit double precision.

The Model 1664's executive mode provided hardware protection between user programs and between user and executive systems in a multiprogrammed environment.

Total memory addressability was 512K bytes in the Model 1664 with main memory available in 16K byte increments. Up to 64K bytes of 1 microsecond core memory could have been installed in a memory chassis attached to the processor. Multiport access to external memory permitted the Model 1664 to operate in a multiprocessor mode with each processor sharing common external memory.

As many as 61 I/O devices were interfaced to the Model 1664. The Model 1664, like the Model 1602, utilized the I/O bus organization to transfer data between the computer and peripheral devices at rates up to 2M bytes per second. [9,15]

B. DATA GENERAL CORPORATION

1. Model 830 Specifications

The Model 830 was a non-militarized medium scale computer with high density core memory, dual operations, and flexible I/O.

The Model 830 operated with a memory management and protection unit allowing memory expansion to 256K bytes, priviledged instructions, protection for I/O devices, and both read and write protection for main memory. Dual operation allows any two major systems programs to run concurrently, each with full protected access to systems resources. For example, 32 terminals can time share in BASIC, while a batch stream runs.

The central processor was organized around four 16 bit accumulators of which two could have been used as index registers. The multi-accumulator architecture reduced the number of instructions necessary to execute a program. Full memory cycle time was 1000 nanoseconds, executing arithmetic and logical instructins in one cycle.

The Model 830 used 16 bit, single word, multifunction instructions. For example, arithmetic and

logical instructions, in addition to their eight basic functions, modified an operand, shifted the result, and/or tested the result. Altogether a total of 256 variations could have been performed on each arithmetic and logical instruction. Memory reference instructions moved data between memory and accumulators, and modified program flow. I/O instructions transfer data between accumulators and peripherals, and control those peripherals.

Major subassemblies were packaged on a single printed circuit board. A single etched back panel made all interboard connections. The Model 830 contained two central processor boards, and either contained or was wired for a memory management and protection unit. There were seventeen subassembly slots. The expansion chassis, which was mounted below the computer, had slots for seven I/O boards. The Model 830 was rack mountable. [23]

2. Model 1210 Specifications

The central processor of the Model 1210 was organized around four 16 bit accumulators. The computer had a full memory cycle time of 1.2 microseconds and executed arithmetic and logical instructions in slightly more than one cycle, 1.35 microseconds. Major subassemblies are packaged on a single printed circuit board. A single etched back panel, with an integral power supply, makes all interboard connections. Plug-in connectors are provided for commonly specified peripherals. The Model 1210 contained one central processor board, one memory board, and space for additional memory boards and I/O subassembly boards. The Model 1210 was rack mountable or table top mountable with four subassembly slots.

In general, the Model 1210 was a scaled down version of the Model 830 resulting in less capacity for expansion. [22]

C. SPERRY UNIVAC CORPORATION

1. AN/UYK-20(V) Specifications

The AN/UYK-20(V) manufactured by Sperry Univac was a "militarized", general purpose 16 bit digital computer. It was physically and functionally modular in construction and expandable in nature. The system contained integral blowers and power supply, mountable on a 19 inch rack with plug in options. The entire system would pass through a 25 inch opening.

The central processor was a microprogrammed controller using two's complement arithmetic, 8 or 16 or 32 bit operands and 16 bit general purpose registers. The central processor used either 16 or 32 bit instructions, had direct addressing to 65K words and indexed via general registers. The central processor contained a power fault enabling automatic restart.

Main storage was expandable from 8K to 65K words in 8K increments. The read/restore cycle time was 750 nanoseconds.

The central processor had a MATH PAC option which included floating point, square root, trigonometric and hyperbolic, double precision multiply, and double precision add capabilities.

Cooling was by circulation of ambient air by internal blowers.

Three general purpose fully supported software packages were available. The "level 1" system functions available under operator control from an on-line keyboard consisted of the following major components: core resident routines, library subroutines, loader subsystems, utility subsystems, system tape generators, and a basic assembler. The system operated with a miminum of 16K words of memory, a key board, and a papertape reader/punch. The "level 2" system was a more comprehensive support system than level 1. The major considerations in "level 2" was a CMS-2M compiler which required a minimum of four magnetic tape units for CMS-2M compilations. The third level was a standard real time executive for real time systems. [10,26]

The individual specifications on each system are listed in Appendix A.

APPENDIX D

GLOSSARY OF TERMS

ADPE ..... Automatic Data Processing Equipment
ATAC ..... Applied Technology Airborne Computer
ATR ..... Air Transportable Rack
BPI ..... Bits Per Inch
CFA ..... Computer Family Architecture
CMS-2 ..... Compiler monitoring system-II
ECM ..... Electronic Countermeasures
ECMU ..... Extended Core Memory Unit
EMI ..... Electromagnetic Interference
ECB ..... Electronic Order of Battle
EPL ..... Electronic Parameter List
EW ..... Electronic Warfare
LAMPS DPU . Light Airborne Multi-purpose System Data Processing Unit
LED ..... Light Emitting Device
MTBF ..... Mean Time Between Failure
MTTR ..... Mean Time To Repair
MAGIS ..... Marine Air Ground Intelligence System
NIPS ..... Naval Intelligence Processing System
NTDS ..... Naval Tactical Data System
TERPES .... Tactical Electronic Reconnaissance Processing and Evaluation Segment

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